REMARKS

I. Present Disposition of the Claims:

The Applicants wish to reiterate thanks to the Examiner for considering the December 19, 2002, Amendment after the November 2, 2002, Final Rejection, as well as for the useful comments in the January 28, 2003, Advisory Action. Claims 14, 17, 19 and 21 have been herein preliminarily amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims were allowable as originally filed. A marked-up version of Claims showing the changes made, is herewith submitted. Therefore, reconsideration of the present application in light of the foregoing preliminary amendment and these remarks is respectfully requested.

II. Previous Rejection of Claims 1-5 and 14-21 under 35 U.S.C. §103(a):

In the November 2, 2002, Final Office Action, the Examiner has previously rejected Claims 1-5 and 14-21 under 35 U.S.C. §103(a) as being unpatentable over Su et al. (US 6,133,096), in view of Cho et al. (US 6,027,971), stating:

> ... claims 1, 2, 4, 14, 15, 19, Su ... discloses a semiconductor memory device comprising: a silicon substrate (1) (... col. 3, ll. 38-40) including a peripheral memory region (90) and a core memory region (70); a transistor formed on the peripheral memory region; one set of dual gate core memory structures (15) including a stacked layer arrangement of semiconductor layers (7, 10) and a dielectric material layer (9), the dual gate core memory structure having sidewall portions; sidewall spacer structures (21) of silicon nitride (... col. 6, ll. 13-18) formed on the sidewall portions of [the] dual gate core memory structures (Fig. 7B; Fig. 15).
>
> **Su ... does not explicitly teach that the silicon nitride for forming [the] spacer structures (21) [has] the chemical formula of Si_3N_4.**
>
> Cho ... discloses a semiconductor memory device comprising: a dual gate core memory structure (62) formed in the core memory region; [] sidewall spacer structures (68) formed on sidewall portions of the dual gate core memory structures, **wherein the sidewall spacer structure [is] formed [from] silicon nitride (Si_3N_4). ... obvious ... to form sidewall spacer structures of silicon nitride (Si_3N_4) as taught by Cho ....**
>
> ... inherent that, the sidewall spacer structures in above combined device is also capable [of protecting] the stacked layer arrangement during etching operations and is compatible with ion implantation and salicidation fabrication process[es] as [the] claimed device.
>
> ... claimed properties [or] functions are presumed to be inherent. In re Best, 195 USPQ 430, 433 (CCPA 1977).
>
> The expressions "dual-purpose" and "being used for lithographic patterning for protecting said stacked layer arrangement during etching operations" [in] claims 1, 4, 14, 17, 19, and 21[,] are considered as intended use limitations and are not considered towards patentability. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to [patentably] distinguish the claimed invention from the prior art. ....
>
> ... claims 3, 5, 17, 18, Su ... teaches that the silicon nitride spacer structures (21) being deposited in a thickness of 1000 [Å] (col. 6, ll. 13-18).
>
> ... claims 20 and 21, ... Su ... the silicon nitride spacer also being a pattern formation

structure for at least one peripheral memory element [(Fig. 15)].

In the December 19, 2002, Response to Final Office Action, Claims 1-5 have been canceled, without prejudice, and Claims 14-21 were added to better encompass the present invention. Notwithstanding independent Claims 14, 17, 19, and 21 having been herein preliminarily amended to better encompass the present invention, the Applicants respectfully traverse the Examiner's ground for rejection on this basis. Specifically, the Claims have been amended to recite the ARC materials and their critical thickness range better, and to recite spacing requirements between core memory stacks. As conceded by the Examiner, "Su ... does not explicitly teach that the silicon nitride for forming [the] spacer structures (21) [has] the chemical formula of Si_3N_4." Su merely teaches (col. 6, ll. 13-18): "**Insulator spacers 21**, comprised of **silicon nitride**, are next formed on the sides of the gate structure, in peripheral device region 90, and on the sides of stacked gate structures 15, in flash memory cell region 70 ... **at a thickness between about 1000 to 2500 Angstroms**, ..." [**Emphasis added**.] Su's spacer 21 is, thus, too thick to provide the presently claimed anti-reflectance capability. As such, Su does not teach, suggest, nor motivate the presently claimed ARC materials (i.e., **SiON, stoichiometric Si_3N_4, or SiGe** in the Markush group) nor the presently claimed **thickness range from 300 Å up to 1000 Å.**

The Examiner has combined Cho with Su to show stoichiometric silicon nitride (Si_3N_4) as a sidewall material: "Cho ... discloses a semiconductor memory device comprising: a dual gate core memory structure (62) formed in the core memory region; [] sidewall spacer structures (68) formed on sidewall portions of the dual gate core memory structures, wherein the sidewall spacer structure [is] formed [from] silicon nitride (Si_3N_4) ... obvious ... to form sidewall spacer structures of silicon nitride (Si_3N_4) as taught by Cho ...." Cho merely teaches (col. 4, ll. 40-43): "... the **insulating spacers 68** are preferably formed of a material having a large etching selectivity relative to silicon dioxide, such as a nitride material, including **silicon nitride (Si_3N_4) and silicon oxynitride (SiON)**." [**Emphasis added**.] Cho does **not** teach any thickness range at all for the spacers 68. As such, Su, even in view of Cho, does not teach, suggest, nor motivate the presently claimed ARC materials (i.e., **SiON, stoichiometric Si_3N_4, or SiGe** in the Markush group) nor the presently claimed **thickness range from 300 Å up to 1000 Å.**

In contrast to Su, in view of Cho, the present invention teaches and claims **a sidewall spacer structure 18** comprising **an anti-reflective coating material** for protecting said stacked

layer arrangement during etching operations, **wherein said anti-reflective coating material comprises a material selected from a group consisting of *silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe)***, said group being compatible with ion implantation and salicidation fabrication processes, and **wherein said anti-reflective coating material comprises a thickness ranging from *300 Å up to 1000 Å*** and also comprises a pattern formation structure for said at least one peripheral memory element as fully supported by the Specification (p. 4, ll. 1-25). Neither Su nor Cho teach the use of **SiGe** as a spacer material at all. As such, the present invention claims Markush species (i.e., **SiON, stoichiometric Si_3N_4, and SiGe**) as well as a **critical thickness range (i.e., ≥300 Å and <1000 Å)** which are not taught, suggested, nor motivated by Su, even in view of Cho. For anti-reflection or optical absorption, only the present invention spacers 18 provide the critical thickness range. While Su and Cho disclose typical, thick spacers, such spacers do not provide the superior absorption capability as do those of the present invention (i.e., not all spacers are created equally).

Specifically, the physics of the present invention may be described as follows:[1]

> No material is perfectly transparent; as light passes through any optical medium (except vacuum) its energy is partially absorbed, increasing the internal energy of the material, and the intensity (power per unit area) is correspondingly attenuated.
>
> **When a beam of light passes through a *thin* sheet of material, of thickness *dx*, the decrease *dI* in its intensity *I* is found to be proportional to the initial intensity *I* and to the thickness *dx*.** Thus[,]
>
> $$dI = -\alpha I dx. \qquad (38\text{-}6)$$
>
> The proportionality constant α, which depends on the material, is called the *absorption coefficient*. The intensity after passage through a slab of finite thickness x can be obtained by integrating Eq. (38-6):
>
> $$I = I_0 e^{-\alpha x}, \qquad (38\text{-}7)$$
>
> where I_0 is the intensity at x = 0. Equation (38-7) is called *Lambert's law*. [Emphasis added.]

This being so, where the initial intensity and the absorption coefficient are constant, by lowering the coating thickness (i.e., *dx* decreasing), the intensity is also lowered (i.e., *dI* decreasing), because *dI* is directly proportional to *dx* (Eq. 38-6). Conversely, if the thickness increases, so does the intensity, thereby resulting in undesirable reflectance, the very problem

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1. Francis W. Sears, Mark W. Zemansky, and Hugh D. Young, University Physics, 5th Ed., pp. 648-649, Addison-Wesley Publishing Company (June 1980).

illustrated by the cited art for which the present invention provides a solution. Further, the thickness for minimizing specular reflectance (i.e., maximizing absorption) may be expressed as follows:[2] $t = m/[2(n^2-\sin^2 f)^{1/2}Dn]$, where m = number of fringes, n = the refractive index, f = the incident angle, and Dn = the wavenumber span (wavenumber = 1/wavelength). Consequently, the Applicants have claimed their critical thickness range **(i.e., ≥300 Å and <1000 Å)** in combination with their claimed ARC materials (i.e., **SiON, stoichiometric Si_3N_4, and SiGe**) for providing a spacer material 18 having **superior optical absorption** capability, *during photoresist processing as well as during subsequent ion implantation and salicidation fabrication processing.*

In particular, only the present invention comprises an ARC which approaches total internal reflection as given by the following equation derived from Huygen's Principle and Snell's Law:[3] $\sin \phi_{crit} = n_b/n_a$, where n_b = the refractive index of the medium through which the incident light (wave front) travels prior to entering the ARC (e.g., $n_b = 1$ in the case of air)[4], n_a = the refractive index of the ARC itself (e.g., $n_a \simeq 1.5$ for SiON, $n_a \simeq 2.0$ for Si_3N_4, and $n_a \simeq 3.4$ to 4.0 for SiGe depending on exact stoichiometry)[5,6,7], and ϕ_{crit} = the critical angle at which total internal reflection occurs. Sears et al. further explain: "Total internal reflection can occur only when a ray is incident on the surface of a medium whose index is smaller than that of the medium in which the ray is traveling."[8]

Further, Sears et al. explain destructive interference for thin films: "It follows that if the film thickness is 1/4 wavelength in the film (normal incidence is assumed), the light reflected

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2. www.piketech.com: "Film Thicknesses and Composition," Pike Technologies website, (December 16, 2002).

3. Sears et al., pp. 657-658.

4. *Id.*, at 657.

5. www.ads.computer.org/proceedings/pi/0440/0440015abs.html: G. L. Bona et al., "Versatile Silicon Oxynitride Planar Lightwave Circuits for Interconnect Applications," IEEE 6th Annual International Conference on Parallel Interconnects, Anchorage, Alaska, (October 17-19, 1999).

6. www.ai.mit.edu/people/tk/tks/silicon-nitride.html (December 17, 2002).

7. www.ncsr.csci-va.com/ncsr/materials/sige.asp (December 17, 2002).

8. Sears et al., p. 657.

from the first surface [i.e., the ARC surface in the present invention] will be 180 out of phase with that reflected from the second [i.e., the gate polysilicon surface in the present invention], and complete destructive interference will result. The thickness can, of course, be 1/4 wavelength for only one particular wavelength."[9]

As such, the presently claimed device having the **critical thickness range** allows operation not only during **photoresist development** processes (e.g., using ultraviolet light either in the **UV ultraviolet wavelength range of 100 nm to 250 nm** or the **DUV wavelength range of 4 nm to 100 nm**)[10] ***but also*** during **ion implantation and salicidation** (e.g., using laser light in the **violet visible range of about 420 nm** for nitrogen E-beam or ion-beam laser)[11], wherein the present invention advantage lies. Typically, low-energy laser-beams are used for alignment marking[12], ion-beam lasers for defect repair[13], inspection[14], and package marking[15]. Thus, the present invention ARC protects the device during any subsequent processing steps using a UV source as well as a low-end visible range low-energy laser.

The present invention, comprising an ARC in the claimed critical thickness range (**≥ 300 Å and <1000 Å, i.e., ≥ 30 nm and <100 nm**), when practiced by forming a spacer 18 comprising the ARC at a thickness of 30 nm, **approaches almost complete destructive interference in the low-end UV range or the high-end DUV range**, because **the claimed low-end ARC thickness of 30 nm is approximately equal to 1/4 of the low-end UV wavelength or the high-end DUV wavelength of 100 nm**, which would then be 25 nm. At the other end of the spectrum, so to speak, the present invention, when practiced by forming a spacer 18 comprising the ARC at a thickness of <100 nm, **also approaches almost complete destructive interference in the low-end laser range**, because **the claimed high-end ARC thickness of**

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9. Sears et al., pp. 715-716.

10. Peter Van Zant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing," 4th Ed., p. 205 (McGaw-Hill, 2000).

11. CRC Handbook, p. 10-222.

12. Van Zant, p. 236.

13. *Id.*, at 277.

14. *Id.*, at 451.

15. *Id.*, at 580.

<100 nm is approximately equal to 1/4 of the low-end nitrogen ion beam laser wavelength of 420 nm, which would then be 105 nm).

Consequently, the Applicants respectfully submit that the claimed spacer 18 (ARC) thickness (i.e., thinness, "less is more" in the present invention) range **(≥ 300 Å and <1000 Å, i.e., ≥ 30 nm and <100 nm)** is not arbitrary; the Applicants have purposefully selected the thickness to form a patentably distinct spacer for many facets of device fabrication. Due to this critical layer thickness, herein amended independent Claims 14, 17, 19, and 21 further recite a "coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching and to provide a pattern for said at least one periphery memory element on said periphery memory region" as fully supported by the Specification (p. 4, ll. 20-25). Figures 4 pictorially illustrates the coating 17 that resides on the periphery memory region 9 and Figure 5 illustrates the formed said at least one periphery memory element 7 and 8 after etching the pattern in the coating 17.

In contrast, Cho merely teaches (col. 6, ll. 7-14): "... a layer of photoresist material 70 is patterned on the substrate, to expose a portion of the field oxide isolation region 52 ... [d]uring this step of patterning the layer of photoresist material 70, the first protection layer 64 and the insulating spacers 68 may also be exposed." Su, even in view of Cho, does not teach, motivate, or suggest the present invention, because Su merely teaches (col. 6, ll. 9-19): "[i]nsulator spacers 21, comprised of silicon nitride, are next formed on the side of the gate structure, in peripheral device region 90, and on the sides of stacked gate structure." Therefore, the present invention with the critical layer thickness in combination with the anti-reflective coating structure, shown in Figure 4, and the resulting periphery gate structure, shown in Figure 5, is not taught, suggested, or motivated by Su, even in view of Cho.

In addition, the present invention **improves the state of the art flash memory cell technology** due to the claimed thin sidewall thickness range **(≥ 300 Å and <1000 Å, i.e., ≥ 30 nm and <100 nm).** As shown in **Exhibit A,** the present invention comprising **300 Å** sidewall spacers disposed one each core memory occupies approximately **600 Å**. In contrast, as shown in **Exhibit B**, the Cho core memory stack, in view of Su, with the smallest taught sidewall spacers, i.e., **1000 Å**, occupy approximately **2000 Å.** Consequently, the present invention decreases the distance occupied by core memory stacks by a factor of 3.33, thereby increasing

the number of flash memory cell per unit substrate area, i.e., creating a denser device.

The pending claims are herein amended to demonstrate the patentably distinct structural limitations which are not taught, motivated, suggested, nor even inherent in the cited art. Thus, Su, even in view of Cho, does not teach, motivate, nor suggest herein amended independent Claims 14, 17, 19, and 21, respectively reciting:

14. **(Twice Amended)** A semiconductor memory device, comprising:
   a. a silicon substrate;
   b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;
   c. a core memory region also delineated on said substrate,
      said core memory region comprising at least one set of dual gate core memory structures thereon formed,
         said dual gate core memory structures at least one pair of core memory stacks, and
      said core memory stacks comprising:
         a semiconductor material; and
         a dielectric material defining respective sidewall portions;
   d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations, said anti-reflective coating material comprising silicon germanium (SiGe); and
   e. **a coating residing on said periphery memory region comprising said anti-reflective coating material wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.**

17. **(Twice Amended)** A semiconductor memory device, comprising:
   a. a silicon substrate;
   b. **a periphery memory region** delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;
   c. a core memory region also delineated on said substrate,
      said core memory region having at least one set of dual gate core memory structures thereon formed,
      said dual gate core memory structures comprising at least one pair of spaced core memory stacks, and
      said core memory stacks comprising:
         a semiconductor material; and
         a dielectric material defining respective sidewall portions;
   d. **a sidewall spacer structure** comprising a anti-reflective coating material for protecting said [stacked layer arrangement] core memory stacks during etching operations, wherein said anti-reflective coating material comprises a thickness ranging from **300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å)**; and
   e. **a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.**

19. **(Twice Amended)** A semiconductor memory device, comprising:
a. a silicon substrate;
b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;
c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising at least one pair of spaced core memory stacks,
and
said core memory stacks comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions;
d. **a sidewall spacer structure** comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,
wherein said anti-reflective coating material comprises silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and
wherein said anti-reflective coating material comprises **a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å)**; and
e. **a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.**

21. **(Twice Amended)** A semiconductor memory device, comprising:
a. a silicon substrate;
b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;
c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising at least one pair of spaced core memory stacks,
and
said core memory stacks comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions;
d. **a sidewall spacer structure** comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,
wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said group being compatible with ion implantation and salicidation fabrication processes, and
wherein said anti-reflective coating material comprises a thickness ranging from **300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å)**; and
e. **a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.**

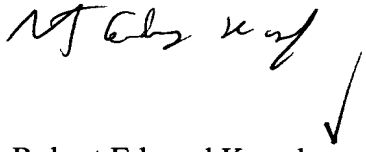
As such, Su, even in view of Cho, does not teach, suggest, nor motivate Claims 15, 16, 18, and 20, now subsuming the limitations of the herein amended independent Claims 14, 17, 19, and

20, now subsuming the limitations of the herein amended independent Claims 14, 17, 19, and 21 and new additions to dependent Claim 15 . Therefore, the Applicants respectfully request that the Examiner's ground for rejection on this basis be withdrawn.

CONCLUSION

Accordingly, without prejudice, Claims 14, 17, 19, and 21 are herein preliminarily amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims would have been allowable as originally filed. Therefore, reconsideration of the present application in light of the foregoing preliminary amendment and these remarks is respectfully requested. ***The Examiner is further cordially invited to telephone the undersigned for any reason which would advance pending claims to allowance.***

Respectfully submitted,



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MARKED UP VERSION OF CLAIMS

In the Claims: Kindly amend Claims 14, 17, 19, and 21 as follows.

14. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery[al] memory region delineated on said substrate, said periphery[al] memory region having at least one periphery[al] memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region [having] comprising at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising [a stacked layer arrangement] at least one pair of core memory stacks, and

said [stacked layer arrangement] core memory stacks comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; [and]

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said [stacked layer arrangement] core memory stacks during etching operations, said anti-reflective coating material comprising silicon germanium (SiGe)[.]; and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

17. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery[al] memory region delineated on said substrate, said periphery[al] memory region having at least one periphery[al] memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising [a stacked layer arrangement]
at least one pair of spaced core memory stacks,
and
said [stacked layer arrangement] core memory stacks comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions; [and]

d. a sidewall spacer structure comprising a anti-reflective coating material for protecting said [stacked layer arrangement] core memory stacks during etching operations, wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and ≺1000 Å) [and also comprises a pattern formation structure for said at least one peripheral memory element.]; and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

19. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery[al] memory region delineated on said substrate, said periphery[al] memory region having at least one periphery[al] memory element thereon formed;

c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising [a stacked layer arrangement]
at least one pair of spaced core memory stacks,
and
said [stacked layer arrangement] core memory stacks comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions; [and]

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said [stacked layer arrangement] core memory stacks during etching operations,

wherein said anti-reflective coating material comprises silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) [and also comprises a pattern formation structure for said at least one peripheral memory element.]; and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

21. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery[al] memory region delineated on said substrate, said periphery[al] memory region having at least one periphery[al] memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising [a stacked layer arrangement] at least one pair of spaced core memory stacks,

and

said [stacked layer arrangement] core memory stacks comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions; [and]

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said [stacked layer arrangement] core memory stacks during etching operations,

wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said group being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from

300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å) [and also comprises a pattern formation structure for said at least one peripheral memory element.]; and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

EXHIBIT A

(Present Invention; Serial No: 06/607,675)

Exhibit A: (Present Invention
Serial No: 06/607,675)

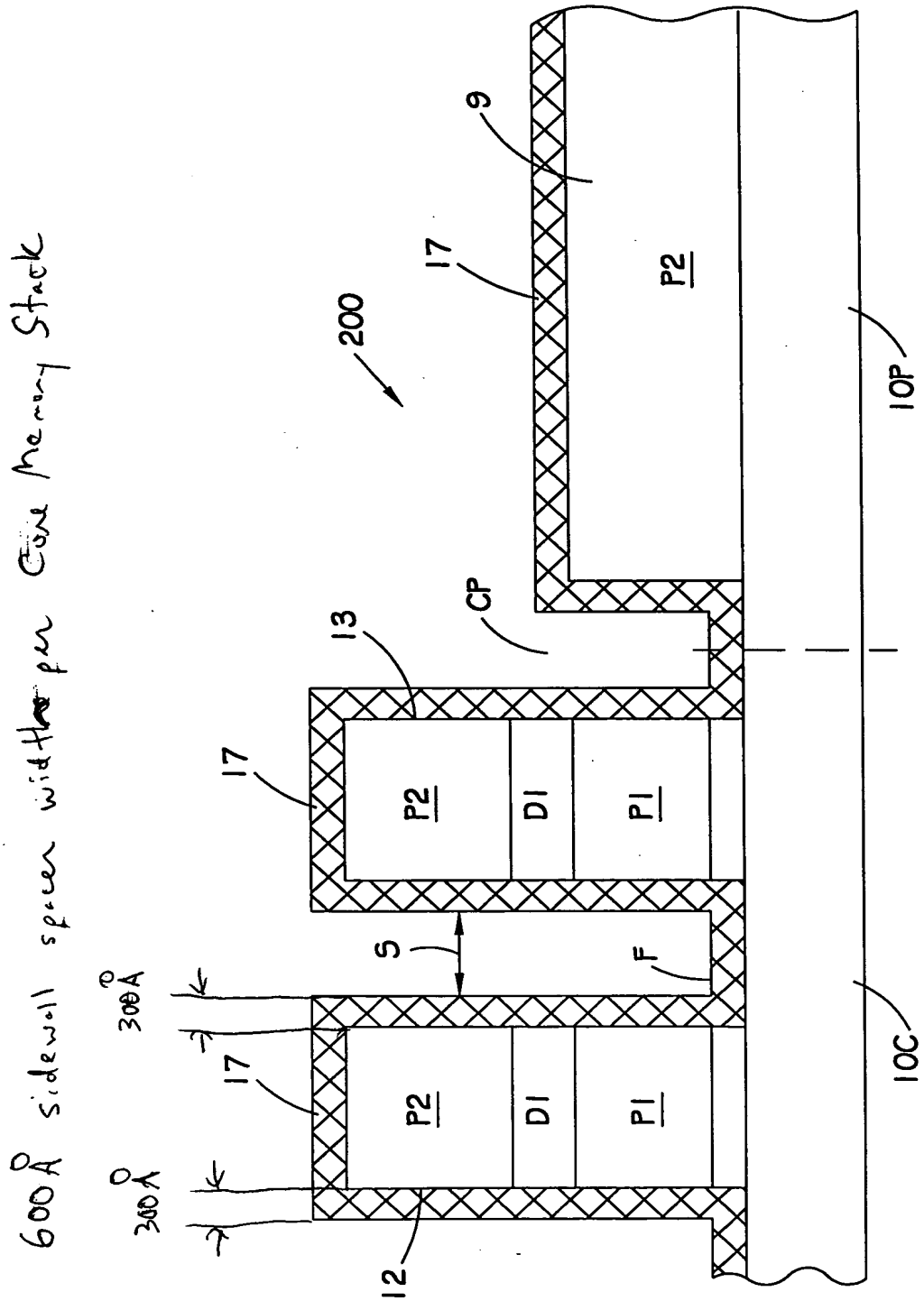

Figure 4.0

EXHIBIT B

(US 6,027,971)

Exhibit B (US 6,027,971)

2000 Å sidewall spacer width per coal memory stack

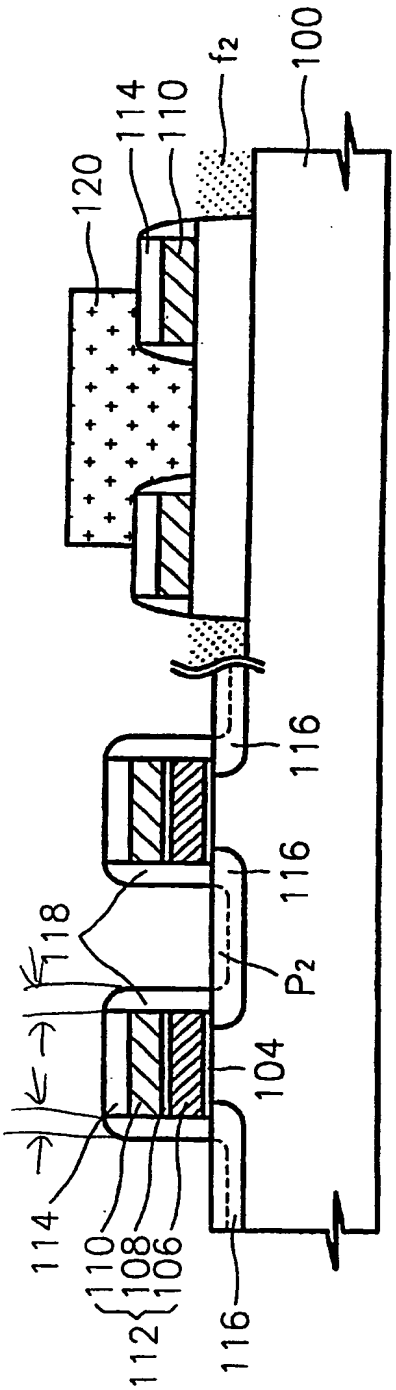

FIG. 16A

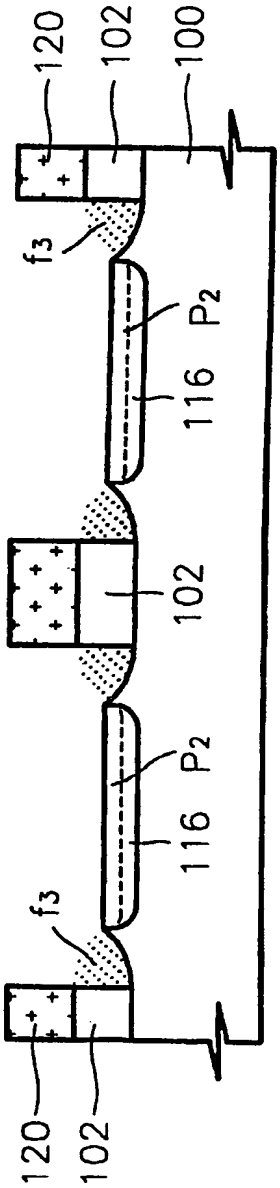

FIG. 16B